Achronix
Data Acceleration

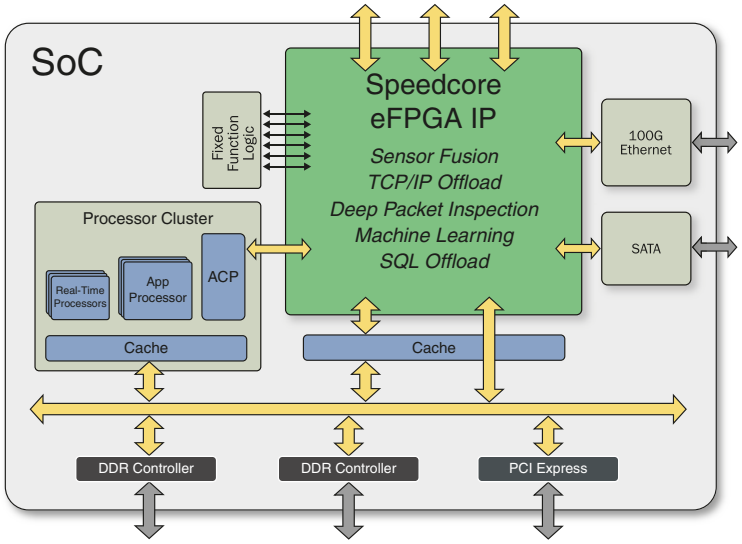
Product Brief

Speedcore eFPGAs

Highlights

- Speedcore™ Embedded FPGA (eFPGA) IP – The only eFPGA technology shipping in high-volume production applications:
  - Customer-defined eFPGA resource counts for logic, embedded memory blocks, MLP and DSP blocks
  - Logic – 6-input look-up-tables (LUTs) plus integrated wide MUX functions and fast adders
  - Logic RAM – 2 kb per memory block for LRAM2k, and 4kb per memory block for LRAM4k
  - Block RAM – 72 kb per memory block for BRAM72k, and 20kb per memory block for BRAM20k
  - DSP64 – 18 × 27 multiplier, 64-bit accumulator and 27-bit pre-adder per block
  - Machine learning processors (MLP) – 32 multiplier/accumulators (MACs) per block, supporting integer and floating point formats
- Achronix delivers the eFPGA IP as a hard macro in GDSII format.
- Speedcore IP is available on the following process technology nodes:
  - TSMC 16FF+
  - TSMC 7nm FinFET
  - TSMC 12FFC under development
  - Speedcore IP can be ported to other process nodes
- Speedcore performance:
  - Max: 750 MHz
  - Typical: 300 MHz to 500 MHz
- Lowest latency interface:
  - One stage of latency between a Speedcore instance and the host SoC
  - Support for zero-latency interfaces
- Speedcore IP supported by Achronix ACE design tools:
  - Full-featured tools to synthesize, place, route and optimize performance for RTL targeting a Speedcore eFPGA
  - Includes Synplify Pro for synthesis
- Easy evaluation:
  - Benchmark designs using Achronix ACE design tools
  - Verify functionality using the VectorPath™ accelerator card

Speedcore eFPGA IP brings the power and flexibility of programmable logic to ASICs and SoCs. Customers specify their logic, RAM, MLP and DSP resource needs, then Achronix configures the Speedcore IP to meet their individual requirements. Speedcore look-up-tables (LUTs), RAM, MLP and DSP64 blocks can be assembled like building blocks to create the optimal programmable fabric for any given application. A personalized version of the ACE design tools to program the Speedcore IP is included with the Speedcore IP delivery.

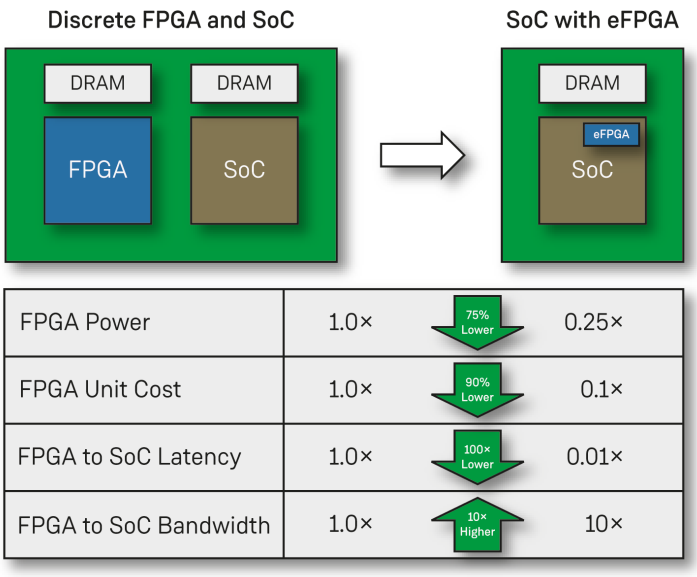


Speedcore High-Level Block Diagram

Speedcore eFPGA technology has been in production and shipping to end customers since 2016. Achronix's customers include some of largest technology companies in the world. These companies have recognized that Speedcore IP is disruptive technology that allows them to dramatically increase the overall performance of their systems.

There are many benefits to embedding Speedcore technology into an SoC. Compared to a separate standalone FPGA, Speedcore eFPGA IP offers the following:

- 75% lower power
- 90% lower cost
- 100× lower latency
- 10× higher bandwidth



Speedcore eFPGAs Minimize Footprint, Improve Performance, Lower Power, Decrease Cost and Future-Proof SoC Designs.

Proven Technology

The cost and risk of building an SoC is too high to gamble with unproven embedded IP. Achronix is the only company shipping both eFPGAs and standalone FPGAs in high-volume production. Designers can be 100% confident that Speedcore IP will work correctly because it has been fully verified and is silicon proven.

Process Technology

Speedcore IP is available in TSMC's 7nm FinFET and 16nm FFT+ process nodes. For other process technologies, Achronix can easily port Speedcore IP to support these requirements. Contact Achronix for more details on porting Speedcore technology.

Evaluating Speedcore eFPGA

Achronix makes it easy to evaluate Speedcore technology before committing to its deployment in an SoC:

1. Achronix ACE design tools can be used to compile designs with an example instance of a Speedcore eFPGA to evaluate performance, resource usage and compile times.
2. Achronix uses its Speedcore Die Size Builder tool to estimate the eFPGA instance size.
3. Evaluation designs can be loaded into the Achronix VectorPath acceleration card to verify functionality and performance.

Moreover, Speedcore IP comes with over a thousand pages of detailed documentation to assist in integrating the technology into your SoC. Achronix also offers several on-site tutorials:

- Benchmarking and evaluation
- Physical design implementation
- Clock and reset network design
- Timing closure
- Configuration
- Verification

Speedcore Supports a Range of Applications

In addition to the straightforward physical advantages of embedding Speedcore technology in complex devices, designers are adding unique, long-term value to their SoC designs. Speedcore IP cores serve as reconfigurable coprocessors and hardware accelerators to support a wide range of tasks that are significantly more efficient on bit-oriented FPGAs compared to word-oriented CPU architectures — functions such as SQL offload engines, inline I/O processing, cryptography, search engine algorithmic acceleration, compression, and enhanced multimedia processing. The range of applications in production or currently being implemented by SoC designers using Speedcore IP continues to expand.

About Achronix

Achronix Semiconductor Corporation is a privately held, fabless semiconductor corporation based in Santa Clara, California and offers high-performance FPGA solutions.

Achronix offerings include programmable FPGA fabrics, discrete high-performance and high-density FPGAs with hardwired system-level blocks, datacenter and HPC hardware accelerator boards, and best-in-class EDA software supporting all Achronix products.

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